

3 has at least one signal output (OUT), at least one
4 switching element (E1, E2) and at least one circuit unit
5 (SCH),

6 wherein

7 the integrated circuit (IC) has a control unit (ST)
8 which is linked to the signal output (OUT) for testing the
9 potential at the signal output (OUT), and

10 the control unit (ST) is linked to at least one
11 switching element (E1, E2), and

12 the input of the switching element (E1, E2) is linked
13 to an output of the circuit unit (SCH), and

14 the output of the switching element (E1, E2) is linked
15 to the signal output (OUT).

16 17. (new) Circuit arrangement according to claim 16,

17 wherein

18 the control unit (ST) for adapting the signals to be
19 tested to the potential of the signal output (OUT) contains
20 an amplifier (LE1, LE2), and

21 the input of the amplifier (LE1, LE2) is linked to the
22 output of a circuit unit (SCH1),

23 the output of the amplifier (LE1, LE2) is linked to
24 the input of the switching element (E1, E2),

25 the control unit (ST) contains at least two
26 comparators (I1, I2 and I3, I4) which form a window
27 discriminator,

28 and has a logic gate (L1, L2) for performing a logic
29 operation on the test signals (SW1, SW2) and at least one
30 more signal (OS) of the circuit unit (SCH),

31 the input of the window discriminator is linked to the